EASWARI ENGINEERING COLLEGE

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

CONNECTRIX

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VISION OF THE DEPARTMENT

To impart quality education in the field of computer science and engineering and to provide graduates with technical skills enabling them to contribute to the society by solving real world problems and to become a centre of excellence for advanced computing.

MISSION OF THE DEPARTMENT

M1. To provide strong foundation in computer science and engineering and in problem solving techniques to become successful professionals in the field of computing and prepare them for higher education.

M2. To provide students with latest skills in the field of computer science and engineering and to realize the importance of life-long learning.

M3. To produce graduates with the ability to participate in interdisciplinary collaborations and apply recent computing tools and technologies in new domains and industry.

M4. To produce graduates capable of ethically and responsibly approaching and committing themselves to the social impact of computing.

M5. To prepare students to communicate effectively and exhibit leadership qualities to work on diverse project teams.

M6. To provide research environment for students and faculty to undertake inter-disciplinary research in emerging areas.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

PEO 1 Graduates will possess the ability to think logically and have capacity to understand technical problems and to design optimal solutions for a successful career in industry, academia and research.

PEO 2 Graduates will have foundation in mathematical, scientific and computer science and engineering fundamentals necessary to formulate, analyze and solve engineering problems.

PEO 3 Graduates will have the potential to apply their expertise and current technologies across multiple disciplines to solve real world challenges and research issues.

PEO 4 Graduates will have the ability to work as a team and will be able to promote the design and implementation of products and services with an understanding of its impact on economical, environmental, ethical, and societal considerations through their strong interpersonal skills, leadership quality and entrepreneurial skills.

PEO 5 Graduates will possess an urge to learn continuously and to be responsive to the demands of the progressive industrial world by carrying out researches in frontier areas of computer science and engineering.

Message from the HOD's Desk

I*t's a great privilege for me to welcome you all for this Academic Year (2018-2019) Even Semester. I congratulate our staff members for their persistent endeavor to make the previous semester a grand success and expecting their extended effort for this semester also. I take this opportunity to encourage our potential talents to excel in academics and also to be aware of the recent trends and current cutting edge technologies to cater them for industrial standards. My heartfelt wishes to each one of you to become successful in all your endeavors. We always look forward to support your academic and personal success.*

"**It always seems impossible until it is done**"

Dr.K.M.Anandkumar
Professor & Head,
Dept. of CSE.

FACULTY ACHIEVEMENTS:

FACULTY FDP ATTENDED:

a. Dr. G.S. Anandha Mala has attended a AICTE sponsored Faculty development Program on the title "**Student Induction Programme**" organized by Easwari Engineering College, Ramapuram from 15.11.2018 to 17.11.2018.

b. Mrs. V. Mercy Rajaselvi, Associate Professor, has attended a Faculty development Program on the title "**Deep Learning**" organized by SRM Institute of Science & Technology, Ramapuram from 22-11-2018 & 23-11-2018.

c. Mr. K.P.K Devan, Associate Professor, has attended a AICTE sponsored Faculty development Program on the title "**Student Induction Programme**" organized by Easwari Engineering College, Ramapuram from 15.11.2018 to 17.11.2018.

d. Dr S. Sobitha Ahila, Associate Professor, has attended a Faculty development Program on the title "**Cyber Forensics**" organized by Panimalar Institute Of Technology from 29-11-2018 & 30-11-2018

e. Mrs. S.Kalpana Devi, Assistant Professor (Sr.G), has attended a Faculty development Program on the title "**Goal Setting**" organized by Aarupadai Veedu Institute of Technology from 22-11-2018 & 23.-11-2018.

f. Mr. P. Hari Kumar, Assistant Professor, has attended a AICTE sponsored Faculty development Program on the title "**Student Induction Programme**" organized by Easwari Engineering College, Ramapuram from 15.11.2018 to 17.11.2018.

g. Mrs.A.Geetha, Assistant Professor, has attended a Faculty development Program on the title "**Goal Setting**" organized by Aarupadai Veedu Institute of Technology from 22-11-2018 & 23.-11-2018.

h. Ms.G.Renown Manjuna, Assistant Professor, has attended a Faculty development Program on the title "**Data Science and Big data Analytics**" organized by DMI College Of Engineering from 19-11-2018 to 23-11-2018.

i. Ms.Rathina priya.V, Assistant Professor, has attended a Faculty development Program on the title "**Data Science and Big data Analytics**" organized by DMI College of Engineering from 19-11-2018 to 23-11-2018.

j. Ms.S.Sri Heera, Assistant Professor, has attended a Faculty development Program on the title "**Data Science and Big data Analytics**" organized by DMI College Of Engineering from 19-11-2018 to 23-11-2018.

k. Mrs.M.Bhanumathi, Assistant Professor, has attended a Faculty development Program on the title "**Data Science and Big data Analytics**" organized by DMI College of Engineering from 19-11-2018 to 23-11-2018.

l. Mrs.V.Rekha, Assistant Professor, has attended a Faculty development Program on the title "**Data Science and Big data Analytics**" organized by DMI College of Engineering from 19-11-2018 to 23-11-2018.

m. Mrs V.S.Vidhyalakshmi, Assistant Professor, has attended a Faculty development Program on the title "**Data Science and Big data Analytics**" organized by DMI College of Engineering from 19-11-2018 to 23-11-2018.

n. Mrs V.S.Vidhyalakshmi, Associate Professor, has attended a Faculty development Program on the title "**Cyber Forensics**" organized by Panimalar Institute Of Technology from 29-11-2018 & 30-11-2018

WORKSHOPS:

a. Dr.R.M.Bhavadharini, Associate Professor, has attended a workshop on the title "**Machine Learning**" organized by St.Joseph Institute of Technology from 22-11-2018 & 23-11-2018.

b. Mrs. V. Ranichandra, Assistant Professor, has attended a workshop on the title "**NLP with hands-on Alexa Skill**" organized by SRM Institute of Science & Technology on 30.11.2018.

c. Ms.R.Poorni, Associate Professor, has attended a workshop on the title "**Machine Learning**" organized by St.Joseph Institute of Technology from 22-11-2018 & 23-11-2018.

d. Mrs.D.Amirtha Sughi, Associate Professor, has attended a workshop on the title "**Machine Learning**" organized by St.Joseph Institute of Technology from 22-11-2018 & 23-11-2018.

FACULTY PUBLICATIONS:

a. Mrs. P. Mercy Rajaselvi Beaulah, Department of Computer Science and Engineering, has published a paper titled "**Categorization of Images Using Autoencoder Hashing and Training of Intra Bin Classifiers for Image Classification and Annotation**" in **Journal of Medical Systems**, 2018.

STUDENTS ACHIEVEMENTS:

STUDENTS PLACEMENTS:

Sl No	Companies Visited	No of Students Placed	No of Students Placed
		UG	PG
1.	WIPRO	1	NA
2.	MAINTECH	3	NA
3.	AITHENT	RNA	NA
4.	FACE	RNA	NA
5.	NEWGEN	3	NA
6.	INFOSYS	3	NA
7.	ZILOGIC	RNA	NA
8.	I-LINK	RNA	NA
9.	SOFT SUVA	RNA	NA
10.	FRESHWORKS	1	NA

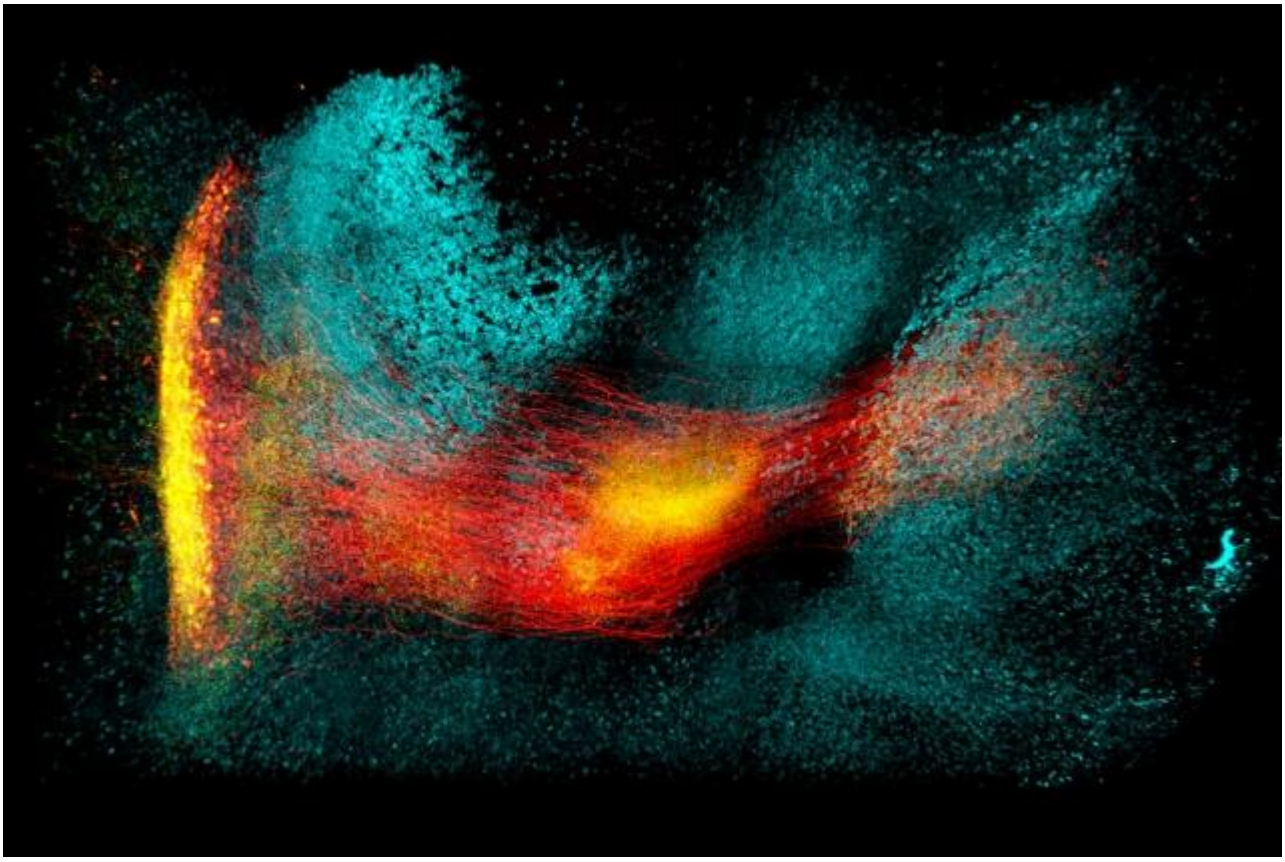
ARTICLES

Mapping the brain, cell by cell

Technique for preserving tissue allows researchers to create maps of neural circuits with single-cell resolution.

MIT chemical engineers and neuroscientists have devised a new way to preserve biological tissue, allowing them to visualize proteins, DNA, and other molecules within cells, and to map the connections between neurons.

The researchers showed that they could use this method, known as SHIELD, to trace the connections between neurons in a part of the brain that helps control movement and other neurons throughout the brain.



"Using our technique, for the first time, we were able to map the connectivity of these neurons at single-cell resolution," says Kwanghun Chung, an assistant professor of chemical engineering and a member of MIT's Institute for Medical Engineering and Science and Picower Institute for Learning and Memory. "We can get all this multiscale, multidimensional information from the same tissue in a fully integrated manner because with SHIELD we can protect all this information."

Chung is the senior author of the paper, which appears in the Dec. 17 issue of *Nature Biotechnology*. The paper's lead authors are MIT postdocs Young-Gyun Park, Chang Ho Sohn, and Ritchie Chen.

Chung is now leading a team of researchers from several institutions that recently received a National Institutes of Health grant to use this technique to produce three-dimensional maps of the entire human brain. "We will be working with the Matthew Frosch group at MGH, the Van Wedeen group at MGH, the Sebastian Seung group at Princeton, and the Laura Brattain group at MIT Lincoln Lab to generate the most comprehensive brain map yet," he says.

PRESERVING INFORMATION:

Brain tissue is very delicate and cannot be easily studied unless steps are taken to preserve the tissue from damage. Chung and other researchers have previously developed techniques that allow them to preserve certain molecular components of brain tissue for research, including proteins or messenger RNA, which reveals which genes are turned on.

However, Chung says, “there is no good method that can preserve everything.”

Chung and his colleagues hypothesized that they might be able to better preserve tissue using molecules called polyepoxides — reactive organic molecules that are often used to produce glues. They tested several commercially available polyepoxides and discovered one that had distinctive structural traits that made it ideally suited for their purposes.

The epoxide they chose has a flexible backbone and five branches, each of which can bind to certain amino acids (the building blocks of proteins), as well as other molecules such as DNA and RNA. The flexible backbone allows the epoxides to bind to several spots along the target molecules, and to form cross-links with nearby biomolecules. This renders individual biomolecules and the entire tissue structure very stable and resistant to damage from heat, acid, or other harmful agents. SHIELD also protects key properties of biomolecules, such as protein fluorescence and antigenicity.

To protect large-scale brain tissues and clinical samples, the researchers combined SHIELD with SWITCH, another technique they developed to control chemical reaction speed. They first use the SWITCH-OFF buffer, which halts chemical reactions, to give the epoxides time to diffuse through the entire tissue. When the researchers move the sample to SWITCH-ON condition, the epoxides begin to bind to nearby molecules.

To speed up the clearing and labeling process of SHIELD-protected tissue, the researchers also applied a randomly changing electric field, which they have previously shown increases the transport rate of the molecules. In this paper, they showed that the entire process from preservation to labeling of biopsy tissue could be performed in just four hours.

"We found that this SHIELD coating keeps proteins stable against harsh stressors," Chung says. "Because we can preserve all the information that we want, and we can extract it at multiple stages, we can better understand the functions of biological components, including neural circuits."
Once the tissue is preserved, the researchers can label a variety of different targets, including proteins and mRNA produced by the cells. They can also apply techniques such as MAP, which Chung developed in 2016, to expand the tissue and image it at different size scales.

In this paper, the researchers worked with Byungkook Lim's group at the University of California at San Diego to use SHIELD to map a brain circuit that begins in the globus pallidus externa (GPe), part of the brain's basal ganglia. This region, which is involved in motor control and other behaviors, is one of the targets of deep brain stimulation — a type of electrical stimulation sometimes used to treat Parkinson's disease. In the mouse brain, Chung and his colleagues were able to trace the connections between neurons in the GPe and in other parts of the brain, and to count the number of putative synaptic connections between these neurons.

BETTER BIOPSIES:

The speed of SHIELD tissue processing means that it also holds promise for performing rapid, more informative biopsies of patient tissue samples, Chung says. Current methods require embedding tissue samples with paraffin, slicing them, and then applying stains that can reveal cell and tissue abnormalities.

“The current way of doing tissue diagnosis hasn’t changed in many decades, and the process takes days or weeks,” Chung says. “Using our technique, we can rapidly process intact biopsy samples and immuno-label them with really specific, clinically relevant antibodies, and then image the whole thing at high resolution, in three dimensions. And everything can be done in four hours.”

In this paper, the researchers showed that they could label mouse kidney tumor with an antibody that targets proliferating cancer cells.
“The stabilization and preservation of biological information within tissue samples is essential in experiments for optical microscopy,” says Liqun Luo, a professor of biology at Stanford University, who was not involved in the research. “The achievement of SHIELD is not a large advance in just one category, but rather marked improvements across the board, in preserving proteins, transcripts, and tissue structure, as samples are processed through the harsh techniques prescribed by today's best labeling and imaging protocols.”

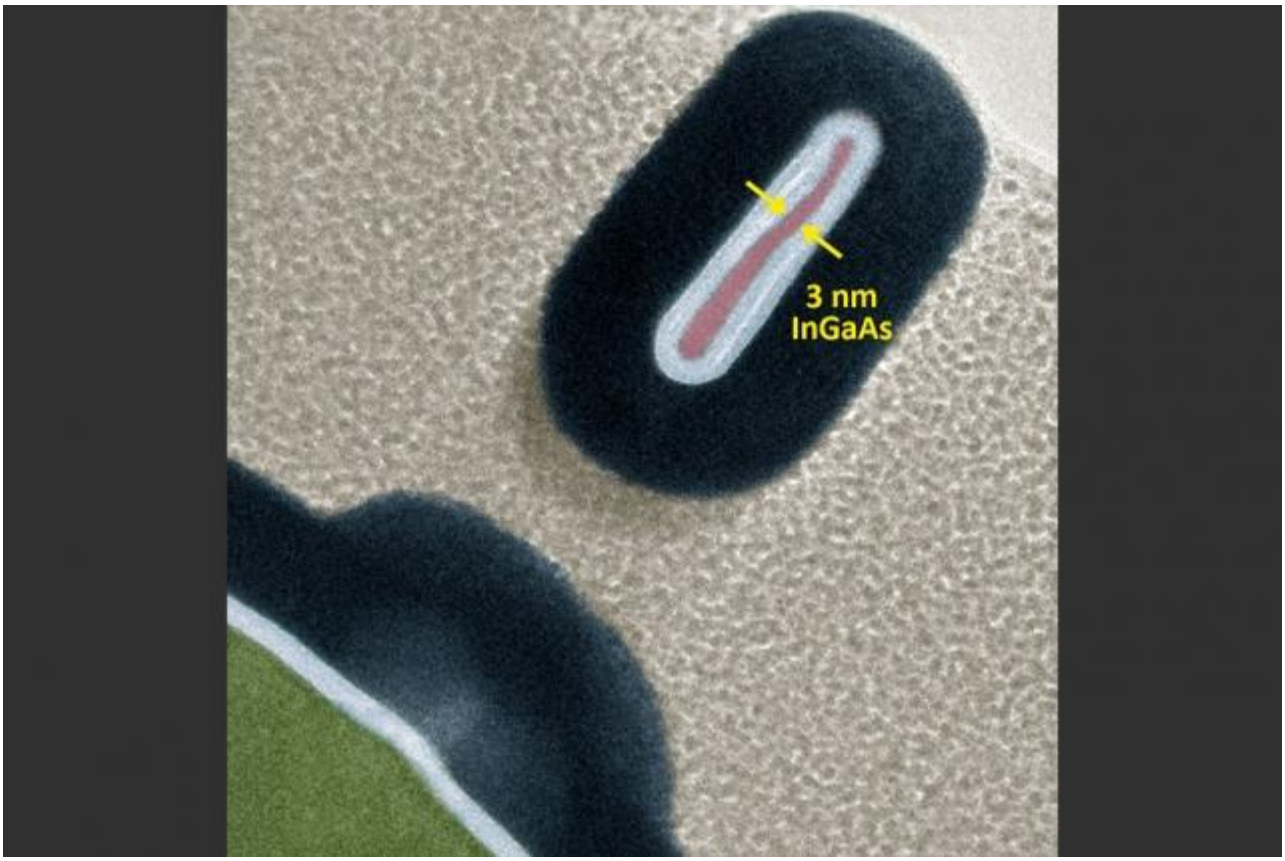
The MIT team hopes to make this technology widely available and has already distributed it to more than 50 labs around the world. The research was funded by the Burroughs Wellcome Fund Career Award at the Scientific Interface, the Searle Scholars Program, the Packard Award in Science and Engineering, the NARSAD Young Investigator Award, the McKnight Foundation Technology Award, the JPB Foundation, and NCSOFT Cultural Foundation, and the National Institutes of Health.

Anne Trafton |
MIT News Office
December 17, 2018

Engineers produce smallest 3-D transistor yet Process that modifies semiconductor material atom by atom could enable higher-performance electronics.

Researchers from MIT and the University of Colorado have fabricated a 3-D transistor that's less than half the size of today's smallest commercial models. To do so, they developed a novel microfabrication technique that modifies semiconductor material atom by atom.

The inspiration behind the work was to keep up with Moore's Law, an observation made in the 1960s that the number of transistors on an integrated circuit doubles about every two years. To adhere to this "golden rule" of electronics, researchers are constantly finding ways to cram as many transistors as possible onto microchips. The newest trend is 3-D transistors that stand vertically, like fins, and measure about 7 nanometers across — tens of thousands of times thinner than a human hair. Tens of billions of these transistors can fit on a single microchip, which is about the size of a fingernail.



As described in a paper presented at this week's IEEE International Electron Devices Meeting, the researchers modified a recently invented chemical-etching technique, called thermal atomic level etching (thermal ALE), to enable precision modification of semiconductor materials at the atomic level. Using that technique, the researchers fabricated 3-D transistors that are as narrow as 2.5 nanometers and more efficient than their commercial counterparts.

Similar atomic-level etching methods exist today, but the new technique is more precise and yields higher-quality transistors. Moreover, it repurposes a common microfabrication tool used for depositing atomic

layers on materials, meaning it could be rapidly integrated. This could enable computer chips with far more transistors and greater performance, the researchers say.

“We believe that this work will have great real-world impact,” says first author Wenjie Lu, a graduate student in MIT’s Microsystems Technology Laboratories (MTL). “As Moore’s Law continues to scale down transistor sizes, it is harder to manufacture such nanoscale devices. To engineer smaller transistors, we need to be able to manipulate the materials with atomic-level precision.”

Joining Lu on the paper are: Jesus A. del Alamo, a professor of electrical engineering and computer science and an MTL researcher who leads the Xtreme Transistors Group; recent MIT graduate Lisa Kong ’18; MIT postdoc Alon Vardi; and Jessica Murdzek, Jonas Gertsch, and Professor Steven George of the University of Colorado.

ATOM BY ATOM:

Microfabrication involves deposition (growing film on a substrate) and etching (engraving patterns on the surface). To form transistors, the substrate surface gets exposed to light through photomasks with the shape and structure of the transistor. All material exposed to light can be etched away with chemicals, while material hidden behind the photomask remains.

The state-of-the-art techniques for microfabrication are known as atomic layer deposition (ALD) and atomic layer etching (ALE). In ALD, two chemicals are deposited onto the substrate surface and react with one

another in a vacuum reactor to form a film of desired thickness, one atomic layer at a time.

Traditional ALE techniques use plasma with highly energetic ions that strip away individual atoms on the material's surface. But these cause surface damage. These methods also expose material to air, where oxidization causes additional defects that hinder performance.

In 2016, the University of Colorado team invented thermal ALE, a technique that closely resembles ALD and relies on a chemical reaction called "ligand exchange." In this process, an ion in one compound called a ligand — which binds to metal atoms — gets replaced by a ligand in a different compound. When the chemicals are purged away, the reaction causes the replacement ligands to strip away individual atoms from the surface. Still in its infancy, thermal ALE has, so far, only been used to etch oxides.

In this new work, the researchers modified thermal ALE to work on a semiconductor material, using the same reactor reserved for ALD. They used an alloyed semiconductor material, called indium gallium arsenide (or InGaAs), which is increasingly being lauded as a faster, more efficient alternative to silicon.

The researchers exposed the material to hydrogen fluoride, the compound used for the original thermal ALE work, which forms an atomic layer of metal fluoride on the surface. Then, they poured in an organic

compound called dimethylaluminum chloride (DMAC). The ligand-exchange process occurs on the metal fluoride layer. When the DMAC is purged, individual atoms follow.

The technique is repeated over hundreds of cycles. In a separate reactor, the researchers then deposited the “gate,” the metallic element that controls the transistors to switch on or off.

In experiments, the researchers removed just .02 nanometers from the material’s surface at a time. “You’re kind of peeling an onion, layer by layer,” Lu says. “In each cycle, we can etch away just 2 percent of a nanometer of a material. That gives us super high accuracy and careful control of the process.”

Because the technique is so similar to ALD, “you can integrate this thermal ALE into the same reactor where you work on deposition,” del Alamo says. It just requires a “small redesign of the deposition tool to handle new gases to do deposition immediately after etching. … That’s very attractive to industry.”

Thinner, better “fins”

Using the technique, the researchers fabricated FinFETs, 3-D transistors used in many of today’s commercial electronic devices. FinFETs consist of a thin “fin” of silicon, standing vertically on a substrate. The gate is essentially wrapped around the fin. Because of their vertical shape, anywhere from 7 billion to 30 billion FinFETs can squeeze onto a chip. As

of this year, Apple, Qualcomm, and other tech companies started using 7-nanometer FinFETs.

Most of the researchers' FinFETs measured under 5 nanometers in width — a desired threshold across industry — and roughly 220 nanometers in height. Moreover, the technique limits the material's exposure to oxygen-caused defects that render the transistors less efficient.

The device performed about 60 percent better than traditional FinFETs in "transconductance," the researchers report. Transistors convert a small voltage input into a current delivered by the gate that switches the transistor on or off to process the 1s (on) and 0s (off) that drive computation. Transconductance measures how much energy it takes to convert that voltage.

Limiting defects also leads to a higher on-off contrast, the researchers say. Ideally, you want high current flowing when the transistors are on, to handle heavy computation, and nearly no current flowing when they're off, to save energy. "That contrast is essential in making efficient logic switches and very efficient microprocessors," del Alamo says. "So far, we have the best ratio [among FinFETs]."

"Thanks to the novel etch technique, this demonstration opens up possibilities for further scaling of transistors with high performance," says Uygar Avci, leader of the Advanced Device Research Group at Intel. "The

work deserves additional praise because of exceptional collaboration of two groups in separate universities with different know-hows: University of Colorado with its material processing innovation and MIT with its transistor design expertise.”

Rob Matheson |
MIT News Office
December 7, 2018