D.Jessintha

Associate.Professor

Contact Information
9566002939

Educational Qualification: M.E

Experience in Easwari : 17 years 10months

Professional Experience : 26 years 9 months

Research Interest: Low Power VLSI Design

Recent Publications:

1. **Jessintha, D**, Kannan, M & Srinivasan, PL 2014, 'Energy Efficient VLSI Based DCT Architecture with Accurate Error Compensation', in Applied Mechanics and Materials doi:10.4028/www.scientific.net/ AMM.626.12, vol. 626, pp. 127-135.(Listed in Annexure II) with an Impact Factor of 0.16

2. **Jessintha, D** & Kannan, M 'Pseudo Pipelined CORDIC DCT Architecture for Image Compression', accepted in the Journal of Computational and Theoretical Nanoscience. (Listed in Annexure I) with an impact factor of 1.42